Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.073”**

**.046”**

**1 16 15**

**14**

**13**

**12**

**11**

**10**

**2**

**3**

**4**

**5**

**6**

**7 8 9**

**MASK**

**REF**

**11645C**

**PAD FUNCTION:**

1. **1A**
2. **1B**
3. **1R**
4. **1Q**
5. **2Q**
6. **2CEXT**
7. **2CEXT/REXT**
8. **GND**
9. **2A**
10. **2B**
11. **2R**
12. **2Q**
13. **1Q**
14. **1CEXT**
15. **1CEXT/REXT**
16. **VCC**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size = .004 x .004”**

**Backside Potential: VCC**

**Mask Ref: 11645C**

**APPROVED BY: DK DIE SIZE .046” X .073” DATE: 7/11/22**

**MFG: HARRIS / TI THICKNESS .014” P/N: 54HC123**

**DG 10.1.2**

#### Rev B, 7/1